IN THE CLAIMS

1. (Currently Amended) A microelectronic device, comprising:

a substrate;

a semi-insulating silicon carbide layer formed on the substrate, the semi-insulating silicon carbide layer comprising boron and a shallow donor impurity, the semi-insulating silicon carbide layer [[and]] having boron-related D-center defects formed therein; and

a first semiconductor device formed on the semi-insulating silicon carbide layer, the first semi-conductor device having an active area comprising a high bandgap material.

2. (Original) The device of Claim 1, wherein the semi-insulating silicon carbide layer is formed epitaxially.

3. (Canceled)

4. (Canceled)

5. (Previously Presented) The device of Claim 2, wherein the first semiconductor device is a high frequency device.

6. (Previously Presented) The device of Claim 2, wherein the first semiconductor device is a high power device.

7. (Original) The device of Claim 1, wherein the substrate is a conductor.

8. (Original) The device of Claim 1, wherein the substrate comprises n^+ silicon carbide.

9. (Original) The device of Claim 1, wherein the semi-insulating silicon carbide layer comprises 6H silicon carbide.

10. (Original) The device of Claim 1, wherein the semi-insulating silicon carbide layer comprises 4H silicon carbide.

11. (Previously Presented) The device of Claim 1, wherein the active area of the first semiconductor device comprises silicon carbide.

12. (Original) The device of Claim 1, wherein the first semiconductor device comprises a metal-oxide-semiconductor field effect transistor.

13. (Currently Amended) The device of Claim 1 ~~Claim 11~~, wherein the first semiconductor device comprises a lateral metal-oxide-semiconductor field effect transistor.

14. (Original) The device of Claim 1, wherein the first semiconductor device comprises a bipolar junction transistor.

15. (Original) The device of Claim 1, wherein the first semiconductor device comprises a junction field effect transistor.

16. (Original) The device of Claim 1, further comprising:

at least a second semiconductor device.

17. (Original) The device of Claim 16, wherein the at least a second semiconductor device is found on a portion of the substrate that is physically isolated from the first semiconductor device.

18. (Original) The device of Claim 16, wherein the at least a second semiconductor device is found on a portion of the substrate that is electrically isolated from the first semiconductor device.

19. (Currently Amended) The device of Claim 1 ~~Claim 11~~, wherein the first semiconductor device is formed epitaxially.

20. (Withdrawn) A method for forming a microelectronic device, comprising:

forming a semi-insulating silicon carbide layer on a substrate; and

forming a first semiconductor device on the semi-insulating silicon carbide layer.

21. (Withdrawn) The method of Claim 20, wherein the substrate is a conductor.

22. (Withdrawn) The method of Claim 21, wherein the semi-insulating silicon carbide layer is formed epitaxially.

23. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide layer comprises boron.

24. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide layer comprises a transition metal.

25. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide is formed using site competition epitaxy.

26. (Withdrawn) The method of Claim 20, wherein forming a semi-insulating silicon carbide layer comprises:

providing a source of silicon;

providing a source of carbon; and

varying a relative concentration of the silicon to the carbon, such that site competition epitaxy occurs.

27. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide layer is formed using boron nitride.

28. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide layer is formed using diborane.

29. (Withdrawn) The method of Claim 20, wherein forming a semi-insulating silicon carbide layer comprises:

supplying a transition metal from a source, wherein the source is selected from a group consisting of a solid source, an organometallic liquid, and a non-organic gas.

30. (Withdrawn) The method of Claim 29, wherein the solid source comprises one selected from a group consisting of vanadium nitride and vanadium carbide.

31. (Withdrawn) The method of Claim 20, wherein forming the semi-insulating silicon carbide layer comprises:

supplying an impurity from a source, the impurity being selected from a group consisting of germanium and chromium.

32. (Withdrawn) The method of Claim 20, wherein the first semiconductor device is formed epitaxially.

33. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide layer has a thickness and a leakage current, the leakage current varying as a function of the thickness and a voltage applied to the microelectronic device.

34. (Withdrawn) The method of Claim 33, wherein the leakage current varies as a function of V2/L3, where V = the voltage applied and L = the thickness of the semi-insulating silicon carbide layer.

35. (Withdrawn) The method of Claim 34, wherein the thickness is at least about 10 micrometers for the voltage of about 350 Volts.

36. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide layer is formed such that the semi-insulating silicon carbide layer has much greater thermal conductivity than a silicon-dioxide layer.

37. (Withdrawn) The method of Claim 20, wherein the semi-insulating silicon carbide layer is formed such that the semi-insulating silicon carbide layer conducts more than 200 times as much heat as a silicon-dioxide layer per unit area.

38. (Currently Amended) An integrated circuit device comprising:

a conducting substrate;

a first semi-insulating silicon carbide layer formed over a portion of the conducting substrate, the first semi-insulating silicon carbide layer being doped with boron and a shallow donor impurity, the semi-insulating silicon carbide layer [[and]] having boron-related D-center defects formed therein;

a first device formed over the substrate; and

a second device formed over the substrate,

wherein the first semi-insulating silicon carbide layer electrically insulates the first device from the second device.

39. (Previously Presented) The integrated circuit device of Claim 38, wherein the first device is formed over the first semi-insulating silicon carbide layer.

40. (Previously Presented) The integrated circuit device of Claim 38, wherein the first device is a high power device.

41. (Previously Presented) The integrated circuit device of Claim 40, wherein the second device is a control device.

42. (Previously Presented) The integrated circuit device of Claim 38, wherein the first device is a high frequency device.

43. (Previously Presented) The integrated circuit device of Claim 42, wherein the second device is a control device.

44. (Previously Presented) The integrated circuit device of Claim 39, wherein the first device is a lateral device.

45. (Previously Presented) The integrated circuit device of Claim 39, wherein the second device is a control device.

46. (Previously Presented) The integrated circuit device of Claim 39, wherein the second device is a vertical device.

47. (Previously Presented) The integrated circuit device of Claim 46, wherein the vertical device is formed over a second semi-insulating silicon carbide layer isolated from the first semi-insulating silicon carbide layer, the second semi-insulating silicon carbide layer being formed over a portion of the conducting substrate different from the portion over which the first semi-insulating silicon carbide layer is formed.

48. (New) The integrated circuit device of Claim 38, wherein the second device is formed over a second semi-insulating silicon carbide layer isolated from the first semi-insulating silicon carbide layer, the second semi-insulating silicon carbide layer being formed over a portion of the conducting substrate different from the portion over which the first semi-insulating silicon carbide layer is formed.

49. (New) The microelectronic device of Claim 1, wherein the shallow donor impurity is nitrogen.

50. (New) The microelectronic device of Claim 1, wherein the semi-insulating silicon carbide layer is formed by epitaxial growth.

51. (New) The microelectronic device of Claim 50, wherein semi-insulating silicon carbide layer is co-doped with boron and nitrogen during epitaxial growth.

52. (New) The integrated circuit device of Claim 38, wherein the shallow donor impurity is nitrogen.

53. (New) The integrated circuit device of Claim 38, wherein the semi-insulating silicon carbide layer is formed by epitaxial growth.

54. (New) The integrated circuit device of Claim 53, wherein the semi-insulating silicon carbide layer is co-doped with boron and nitrogen during epitaxial growth.